

Applicant : Olaf Moeller et al.
Serial No. : 09/770,061
Filed : January 24, 2001
Page : 4 of 10

Attorney's Docket No.: 12754-116001 / 2001P07429US

Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A data processing method, comprising:
receiving one or more combined clock-data streams according to a first clock domain
each combined clock-data stream including both clock and data signals;
dividing ~~said~~ at least one of the one or more combined clock-data streams into ~~at least one~~ an independent clock stream and at least one an independent data stream; and
synchronizing ~~each of said at least one the independent data stream~~ the independent data stream to a ~~common second~~ clocking clock domain for processing by a framer array, the second clock domain being different from the first clock domain; and
preserving a timing of the independent clock stream according to the first clock domain during processing of the independent data stream by the framer array.
2. (Currently Amended) A method in accordance with claim 1, ~~including further~~ comprising:
dividing a plurality of the one or more combined clock-data streams into a plurality of independent clock streams and a plurality of independent data streams; and
multiplexing a the plurality of said at least one independent data streams stream for processing by a the framer array, said the framer array being provided offset a data path of said at least one of the plurality of independent data streams stream.
3. (Currently Amended) A method in accordance with claim 2, further comprising aligning octets of ~~said~~ at least one of the plurality of independent data streams stream onto a

Applicant : Olaf Moeller et al.
Serial No. : 09/770,061
Filed : January 24, 2001
Page : 5 of 10

Attorney's Docket No.: 12754-116001 / 2001P07429US

multiplexed bus, the multiplexed bus being synchronized to said common the second clock
clocking domain.

4. (Currently Amended) A method in accordance with claim 3, further comprising:
demultiplexing said the plurality of at least one independent data streams; stream and
recombining said at least one independent data stream and said at least one independent
clock stream to form a recombined clock-data stream; and
re-synchronizing the recombined clock-data stream to the first clock domain.

5. (Currently Amended) A method according to claim 3 [[4]], said at least one data
stream further comprising inserting status and control information to the independent data stream
while the independent data stream is on the multiplexed bus.

6. (Currently Amended) A data processing system, comprising:
means for receiving a plurality of asynchronous combined clock-data streams according
to a first clock domain, each combined clock-data stream including both clock and data signals;
means for dividing said the plurality of combined clock-data streams into component a
plurality of independent clock streams and a plurality of independent data streams;
means for processing said the plurality of independent data streams in a common second
clock domain, the second clock domain being different from the first clock domain, wherein a
timing of each of the plurality of independent clock streams is preserved according to the first
clock domain during the processing of the plurality of independent data streams; and
means for recombining said component corresponding ones of the plurality of
independent clock data streams and the plurality of independent data streams to form a plurality
of recombined clock-data streams; and
means for re-synchronizing the plurality of recombined clock-data streams to the first
clock domain.

Applicant : Olaf Moeller et al.
Serial No. : 09/770,061
Filed : January 24, 2001
Page : 6 of 10

Attorney's Docket No.: 12754-116001 / 2001P07429US

7. (Currently Amended) A data processing system according to claim 6, ~~said wherein the processing means including~~ includes means for multiplexing the plurality of independent data streams onto a common bus onto which said component data streams are multiplexed.

8. (Currently Amended) A data processing system according to claim 7, ~~said wherein the processing means including~~ further includes a framer state machine offset from said the common bus, the framer state machine adapted to align octets of said component each of the plurality of independent data streams onto said the common bus.

9. (Currently Amended) A data processing system according to claim 8, ~~said wherein the processing means including a framer state machine is further~~ adapted to store a context of a last previous data stream processed and load a context of a current data stream.

10. (Currently Amended) A system, comprising:
a plurality of combined clock-data streams having a timing according to a first clock domain, each combined clock-data stream including both clock and data signals;
a plurality of clock paths adapted to extract clocks from [[a]] the plurality of combined clock-data streams;
a plurality of data paths adapted to receive data portions of said the plurality of combined clock-data streams and provide said the data portions onto a common bus in a common second clock domain, the second clock domain being different from the first clock domain; and
a framer unit state machine offset from said the common bus and adapted to load and store a context for said the data portions in the second clock domain,
wherein the plurality of clock paths preserve the clocks according to the first clock domain during a time that context is loaded and stored for the data portions.

Applicant : Olaf Moeller et al.
Serial No. : 09/770,061
Filed : January 24, 2001
Page : 7 of 10

Attorney's Docket No.: 12754-116001 / 2001P07429US

11. (Currently Amended) A system according to claim 10, ~~said wherein the framer unit state machine~~ is further adapted to identify a start of frames of ~~said the~~ data portions.

12. (Currently Amended) A system according to claim 11, ~~including further~~ comprising a plurality of synchronizers adapted to synchronize each of ~~said the~~ plurality of data paths to ~~said the~~ common bus according to the second clock domain.

13. (Currently Amended) A system according to claim 12, ~~including further~~ comprising a plurality of serial-to-parallel converters coupled to ~~said the~~ plurality of synchronizers and adapted to convert the data portions from serial data into parallel data.

14. (Currently Amended) A system according to claim 13, wherein outputs of ~~said the~~ serial-to-parallel converters are provided to a multiplexer.

15. (Currently Amended) A system according to claim 14, wherein outputs of ~~said the~~ multiplexer are provided to ~~said the~~ common bus and ~~said the~~ framer state machine unit.